REMARKS

The Examiner objected claims 6 and 8 as being dependent upon a rejected based claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The Examiner rejected claims 1, 3, 7 and 12-14 under 35 U.S.C. §102(b) as allegedly being anticipated by Ference *et al.* (US 6,611,050).

The Examiner rejected claims 1, 3 and 7 under 35 U.S.C. §102(e) as allegedly being anticipated by Takao (US 2004/0137701).

The Examiner rejected claims 2 and 4 under 35 U.S.C. §103(a) as allegedly being unpatentable over Takao *et al.* as above in view of Cohen (US 6,903,016).

The Examiner rejected claim 5 under 35 U.S.C. §103(a) as allegedly being unpatentable over Ference *et al.* as above in view of Kawakami (US 2003/0190795).

Applicants respectfully traverse the §102 and §103 rejections with the following arguments.

35 U.S.C. §102

The Examiner rejected claims 1, 3, 7 and 12-14 under 35 U.S.C. §102(b) as allegedly being anticipated by Ference *et al.* (US 6,611,050).

Applicants respectfully contend that Ference does not anticipate claim 1, because Ference does not teach each and every feature of claim 1. For example, Ference does not teach "forming N interconnect layers ... wherein N is a positive integer **greater than one,** ... and wherein the entire continuous etchable block comprises **essentially a same material,**" in step (c) of claim 1 (bold emphasis added). More specifically, Ference, in Fig. 13, column 6, lines 45-49, teaches that there is only one interconnect layer 122 (as cited and argued by the Examiner). In contrast, in claim 1, there is more than one interconnect layer (N is greater than one). Furthermore, even if the layers 120, 122, 124, and 126 in FIG. 13 of Ference are considered interconnect layers for the purpose of anticipating claim 1, there are no two interconnect layers of those layers 120, 122, 124, and 126 whose etchable portions would form **a continuous etchable block which comprises essentially a same material** as claimed in claim 1 (bold emphasis added). This is because any two adjacent layers of the layers 120, 122, 124, and 126 comprise different materials (column 6, lines 32-52). Therefore, the continuous etchable block formed from these two adjacent layers would not comprise the same material as claimed in claim 1. Therefore, claim 1 is not anticipated by Ference.

Furthermore, Ference does not teach the feature "cutting with a laser through the semiconductor border region **via an empty space** of the removed continuous etchable block" in step (e) of claim 1 (bold emphasis added). More specifically, Ference, in Fig. 16b and Fig. 17, column 6, lines 65-67, teaches that the empty space 132b created by removing the continuous

etchable block (the middle portion of the layer 122) is later filled with a conductive material 134. After that, the laser cuts through the semiconductor border region 114 from bottom up (as shown in FIG. 17 of Ference). Therefore, the laser does not cut through the empty space of the removed continuous etchable block (the middle portion of layer 122). Moreover, whether the laser cut through the semiconductor border region 114 from bottom up or from top down, the laser does not cut through the empty space of the removed continuous etchable block (the middle portion of layer 122) because the empty space 132b (Fig. 16b) of the removed continuous etchable block (the middle portion of layer 122) has been filled with conductive material 134b before the cutting with the laser. In contrast, in claim 1, the laser cuts through the semiconductor border region **via an empty space** of the removed continuous etchable block (bold emphasis added).

Based on the preceding arguments, Applicants respectfully maintain that Ference does not anticipate claim 1, and that claim 1 is in condition for allowance.

The Examiner rejected claims 3 and 7 under 35 U.S.C. §102(b) as allegedly being anticipated by Ference *et al.* (US 6,611,050). Since claims 3 and 7 depend from claim 1, which is not anticipated by Ference as argued above, Applicants contend that claims 3 and 7 are likewise in condition for allowance.

Applicants respectfully contend that Ference does not anticipate claim 12, because Ference does not teach each and every feature of claim 12. For example, Ference does not teach the feature "forming ... a filled deep trench ... wherein the semiconductor border region **comprises** the filled deep trench" in step (b) of claim 12 (bold emphasis added). More specifically, Ference, in Fig. 4, teaches that the semiconductor border region 14 is separate from the filled deep trench 18. In contrast, in claim 12, the semiconductor border region comprises the

filled deep trench. Therefore, claim 12 is not anticipated by Ference.

Moreover, Ference does not teach "forming N interconnect layers ... wherein N is a positive integer **greater than one** ... and wherein the entire continuous etchable block **comprises essentially a same material**" in step (c) of claim 12 (bold emphasis added). More specifically, Ference, in Fig. 5, column 4, lines 63-64 and column 5, lines 2-10, teaches that there is only one interconnect layer 22 (as cited and argued by the Examiner). In contrast, in claim 12, there is more than one interconnect layer (N is greater than one). Furthermore, even if the layers 20, 22, 24, 26, and 28 in Fig. 5 of Ference are considered interconnect layers for the purpose of anticipating claim 12, there are no two interconnect layers of those layers 20, 22, 24, 26, and 28 whose etchable portions would form **a continuous etchable block which comprises essentially a same material** as claimed in claim 12 (bold emphasis added). This is because any two adjacent layers of the layers 20, 22, 24, 26, and 28 comprise different materials (from column 4, line 60 to column 5, line 22). Therefore, the continuous etchable block formed from these two adjacent layers would not comprise the same material as claimed in claim 12. Therefore, claim 12 is not anticipated by Ference.

Furthermore, Ference does not teach the feature "cutting with a laser through the semiconductor border region **via an empty space** of the removed continuous etchable block" in step (c) of claim 12 (bold emphasis added). More specifically, Ference, in Fig. 7, column 5, lines 36-38, teaches that the empty space 32b created by removing the continuous etchable block (the middle portion of the layer 22) is later filled with a conductive material 34. Then, the laser cuts through the semiconductor border region 14. Whether the laser cut through the border region from bottom up or from top down, the laser does not cut through the empty space of the removed

continuous etchable block (the middle portion of layer 22) because the empty space 32b (Fig. 6b) of the removed continuous etchable block (the middle portion of layer 22) have been filled with conductive material 34b before the cutting with the laser. In contrast, in claim 1, the laser cuts through the semiconductor border region **via an empty space** of the removed continuous etchable block.

Based on the preceding arguments, Applicants respectfully maintain that Ference does not anticipate claim 12, and that claim 12 is in condition for allowance.

The Examiner rejected claims 13 and 14 under 35 U.S.C. §102(b) as allegedly being anticipated by Ference *et al.* (US 6,611,050). Since claims 13 and 14 depend from claim 12, which is not anticipated by Ference as argued above, Applicants contend that claims 13 and 14 are likewise in condition for allowance.

The Examiner rejected claims 1, 3 and 7 under 35 U.S.C. §102(e) as allegedly being anticipated by Takao (US 2004/0137701).

Applicants respectfully contend that Takao does not anticipate claim 1, because Takao does not teach each and every feature of claim 1. For example, Takao does not teach the feature "forming N interconnect layers ... **directly above the semiconductor border region**...wherein N is a positive integer **greater than one**, ... and wherein the entire continuous etchable block comprises **essentially a same material**" in step (c) of claim 1 (bold emphasis added). More specifically, Takao in Fig. 5, teaches that there is only one interconnect layer 21 (as cited and argued by the Examiner). In contrast, in claim 1, there is more than one interconnect layer (N interconnect layers, wherein N is a positive integer **greater than one**). Moreover, the layer 21 does not teach the "N interconnect layers" of claim 1 because the layer 21 is not **directly above**

the semiconductor border region (the middle region of the silicon layer 10 of FIG. 5 of Takao) as claimed in claim 1 (bold emphasis added). Furthermore, even if the layers 18 and 30 in Fig. 5 of Takao are considered interconnect layers for the purpose of anticipating claim 1, their etchable portions would not form **a continuous etchable block which comprises essentially a same material** as claimed in claim 1 (bold emphasis added). This is because the layers 18 and 30 comprise different materials (paragraphs 59 and 60). Therefore, claim 1 is not anticipated by Takao.

Furthermore, Takao does not teach "cutting with a laser through the semiconductor border region **via an empty space** of the removed continuous etchable block" in step (c) of claim 1 (bold emphasis aded). More specifically, Takao, in Fig. 8B and paragraph [0066], suggests that the glass substrate 13 may be made tapered so that when the laser is cutting from this side of the glass substrate 13, the glass substrate 13 was not cracked. This implies that the laser does not cut through the empty space of the removed continuous etchable block created by removing the middle portion of the layer 18. In contrast, in claim 1, a laser cuts through the semiconductor border region **via an empty space** of the removed continuous etchable block.

Based on the preceding arguments, Applicants respectfully maintain that Takao does not anticipate claim 1, and that claim 1 is in condition for allowance.

The Examiner rejected claims 3 and 7 under 35 U.S.C. §102(b) as allegedly being anticipated by Takao *et al.* (US 2004/0137701). Since claims 3 and 7 depend from claim 1, Applicants contend that claims 3 and 7 are likewise in condition for allowance.

35 U.S.C. §103

The Examiner rejected claims 2 and 4 under 35 U.S.C. §103(a) as allegedly being unpatentable over Takao et al. (US 2004/0137701) in view of Cohen (US 6,903,016). Since claims 2 and 4 depend from claim 1, which is in condition for allowance as argued above, Applicants contend that claims 2 and 4 are likewise in condition for allowance.

The Examiner rejected claim 5 under 35 U.S.C. §103(a) as allegedly being unpatentable over Ference et al. (US 6,611,050) in view of Kawakami (US 2003/0190795). Since claim 5 depends from claim 1, which is in condition for allowance as argued above, Applicants contend that claim 5 is likewise in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicant's representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

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